FIG. 1

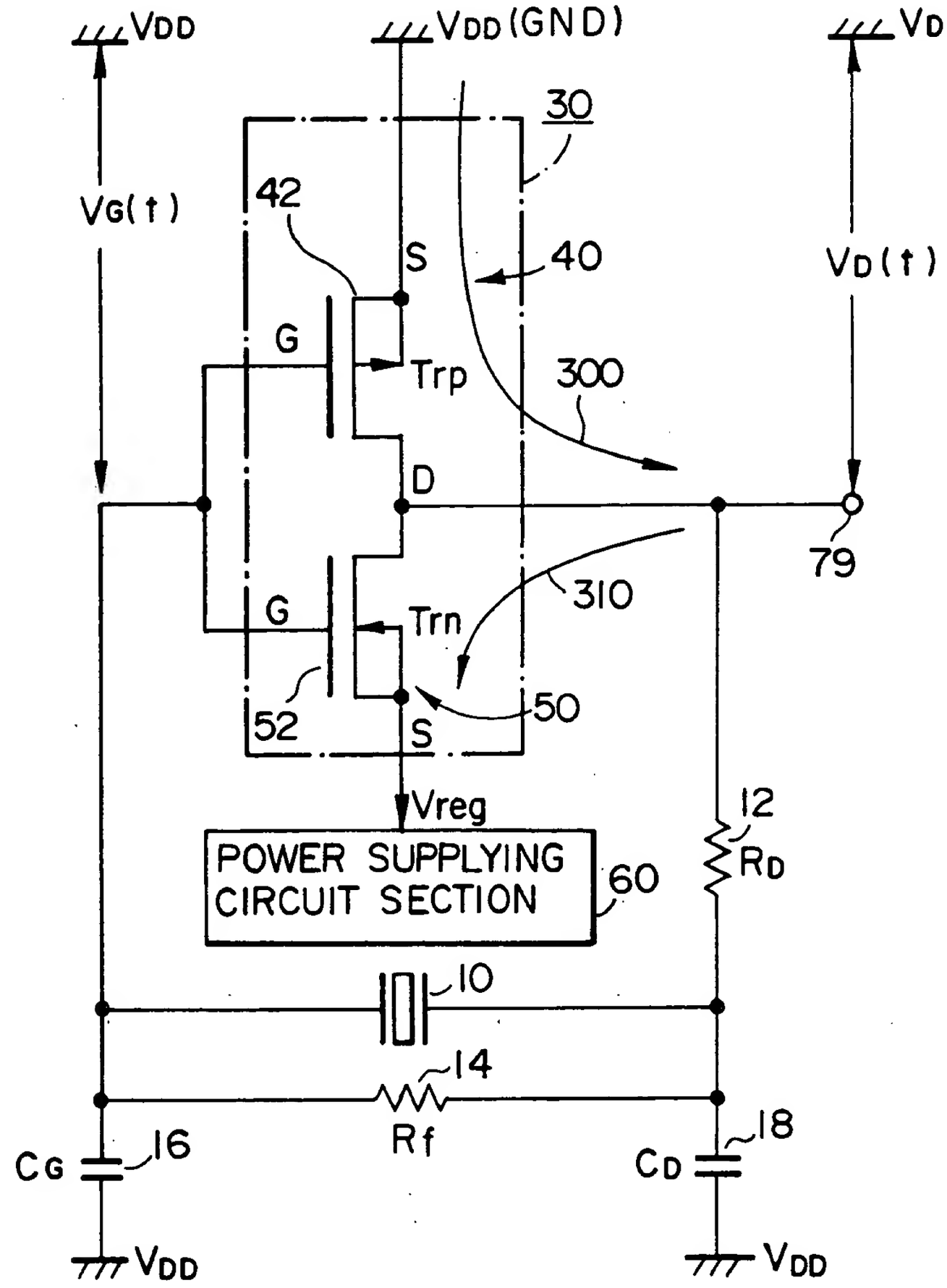

VDD
VDD(GND)
VDD
30
42
S
40
VG(t)
VD(t)
G
Trp
300
D
79
310
G
Trn
52
S
50
Vreg
POWER SUPPLYING CIRCUIT SECTION
60
12
RD
10
14
Rf
CG
16
18
CD
VDD
VDD

FIG. 2
PRIOR ART

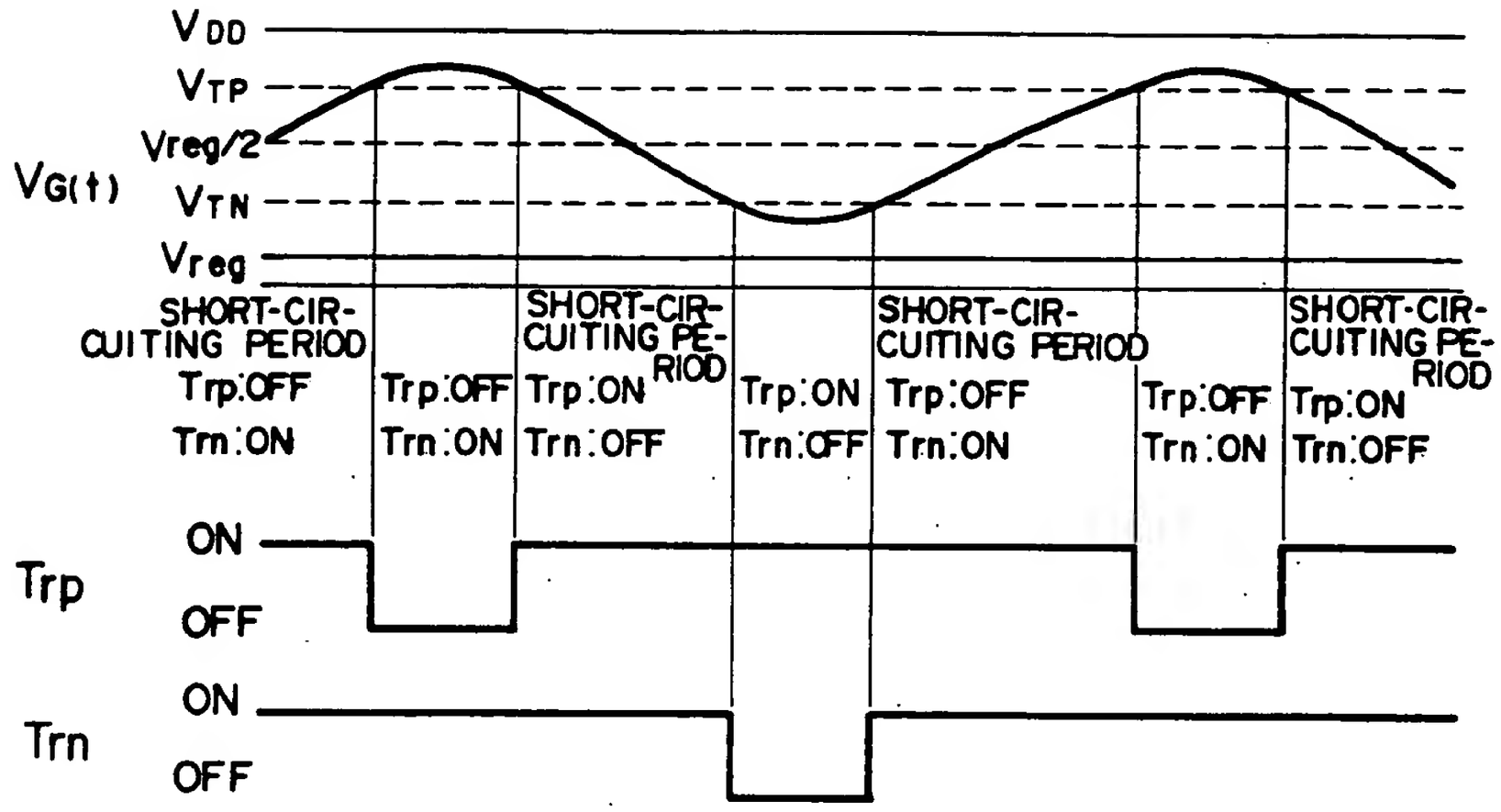


FIG. 3

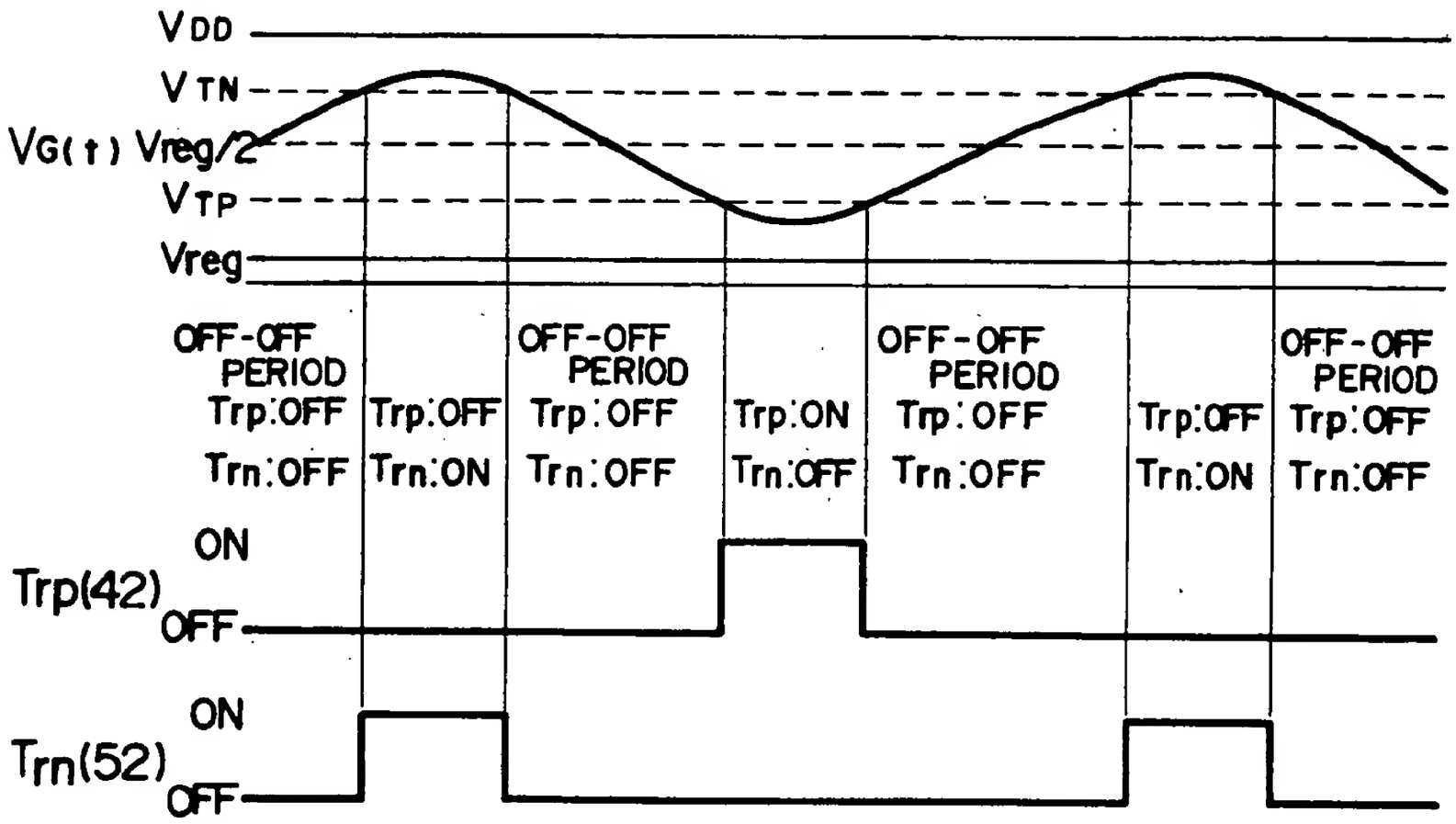


FIG. 4
PRIOR ART

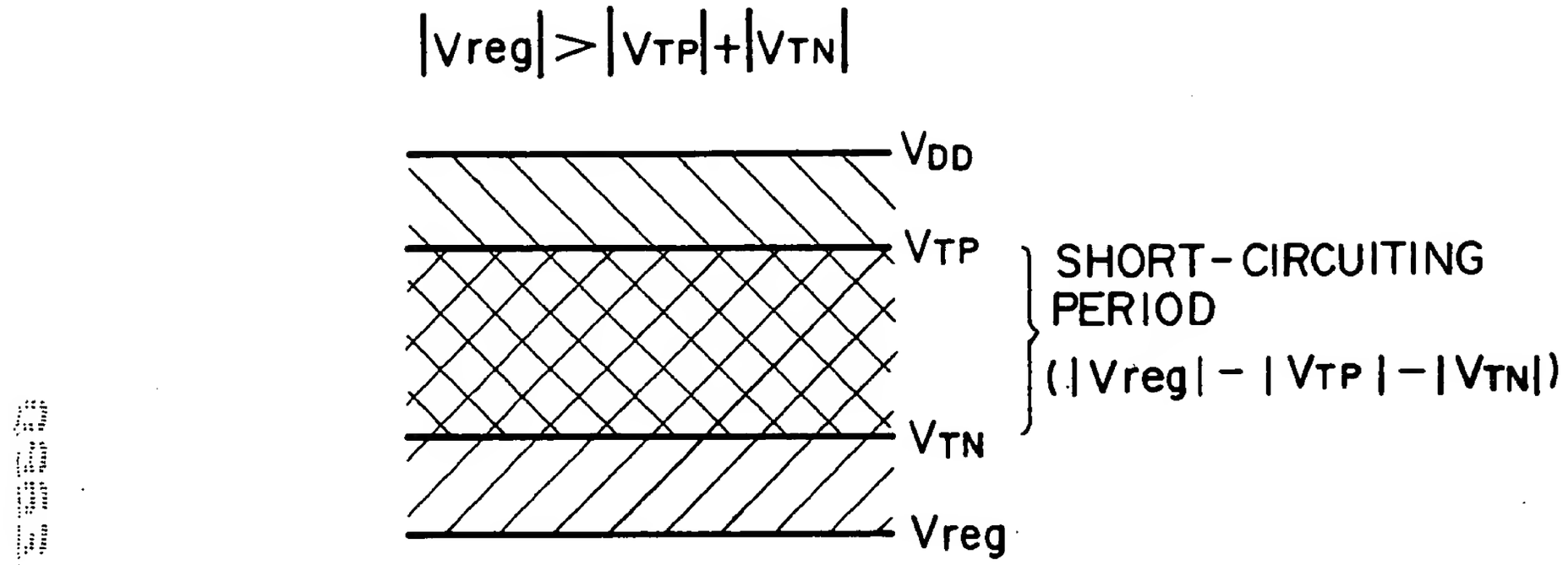


FIG. 5

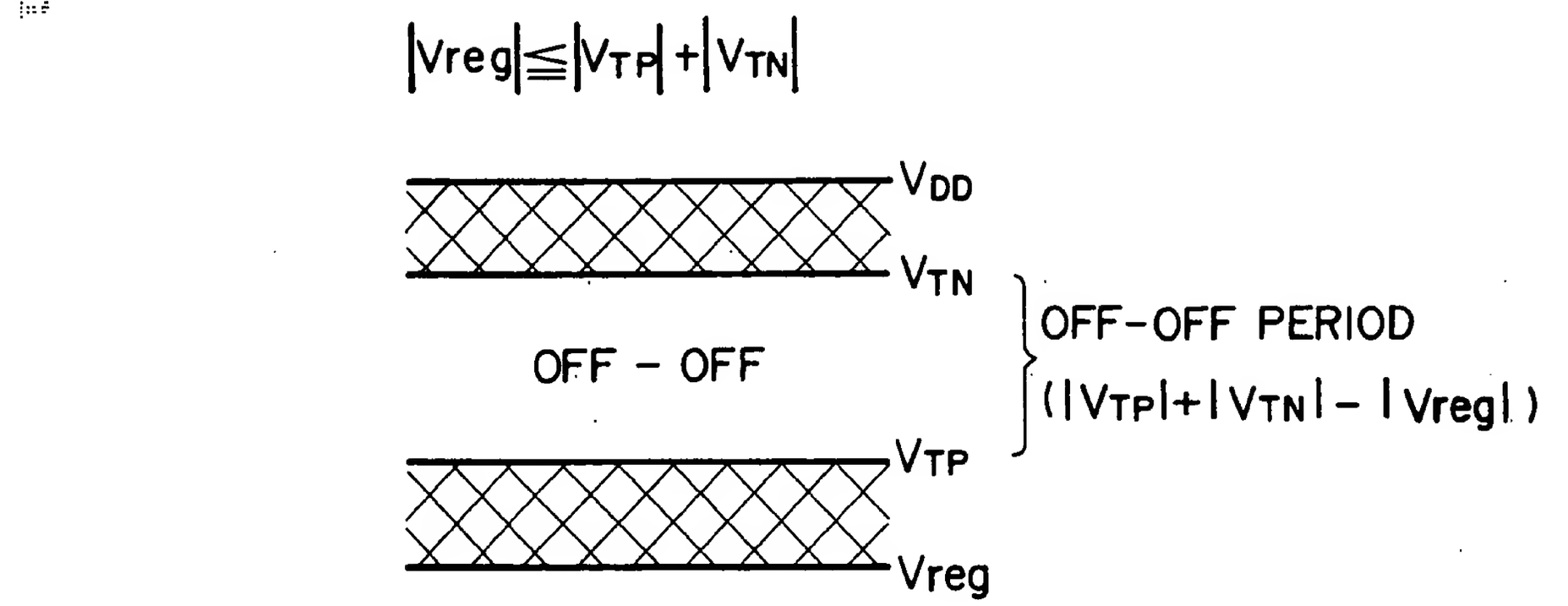


FIG. 6

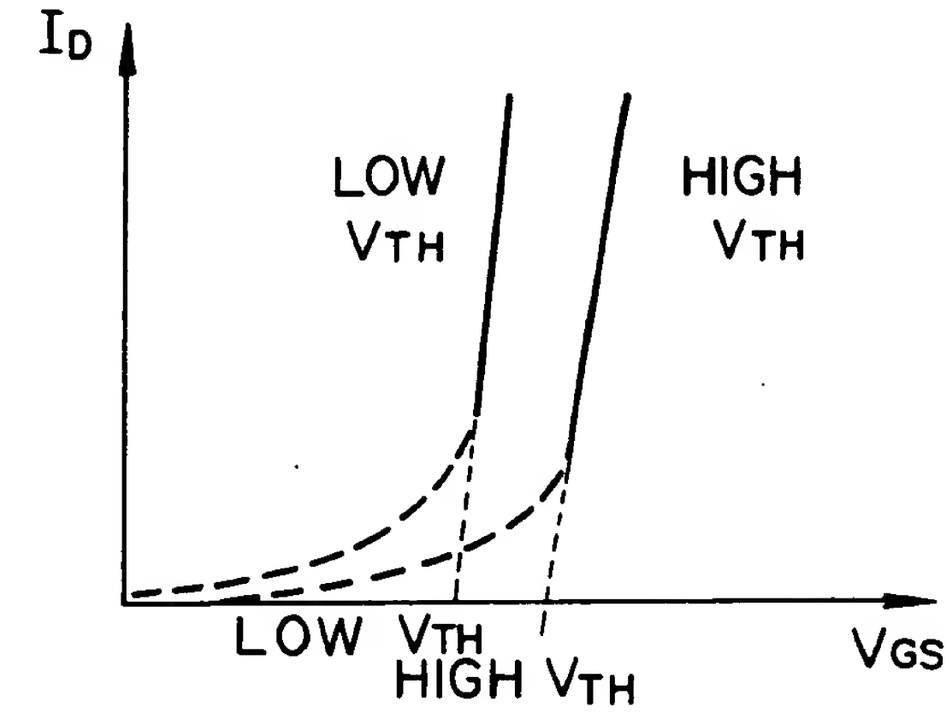

I_D
LOW V_{TH}
HIGH V_{TH}
LOW V_{TH}
HIGH V_{TH}
V_{GS}

FIG. 7

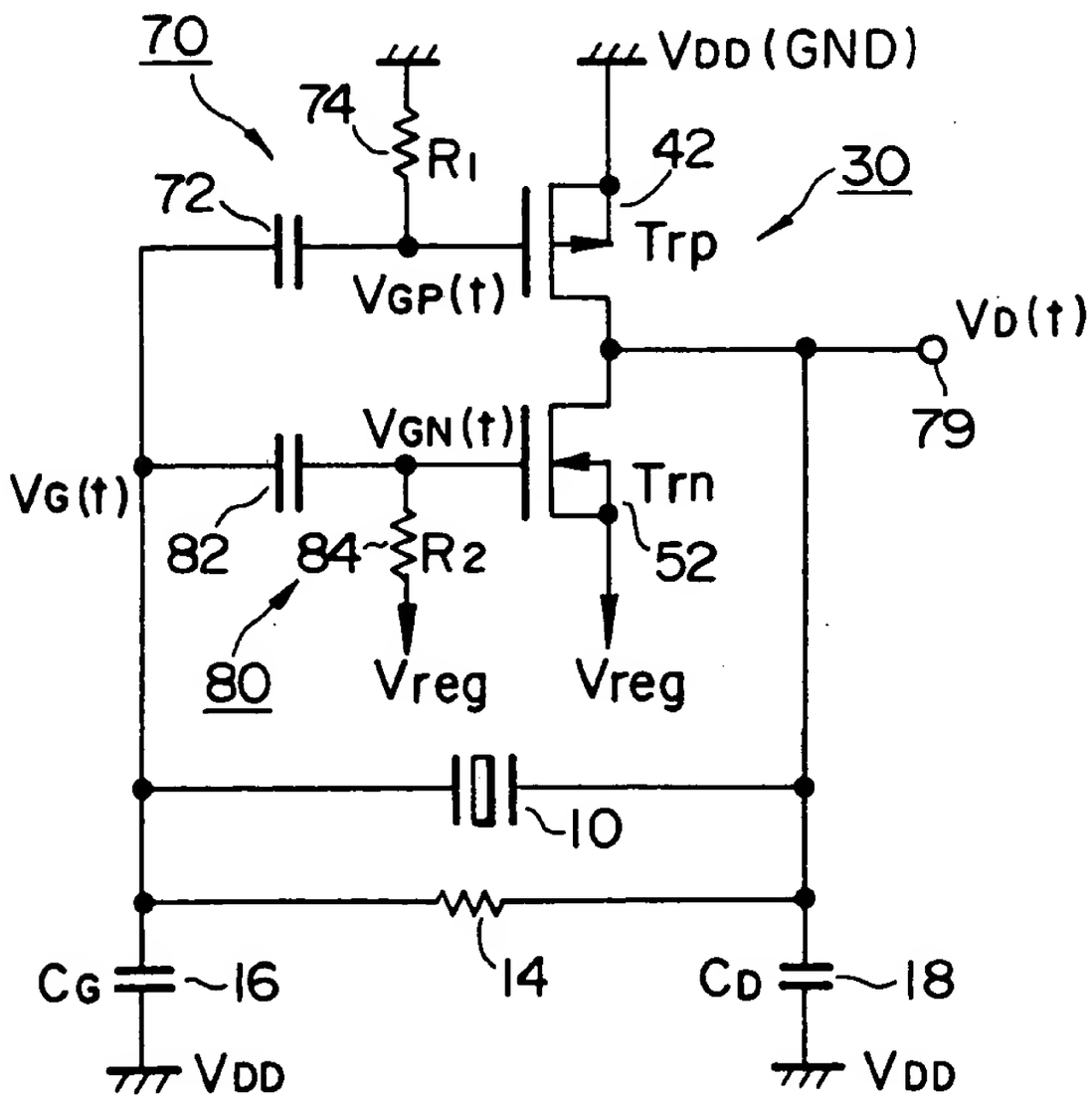
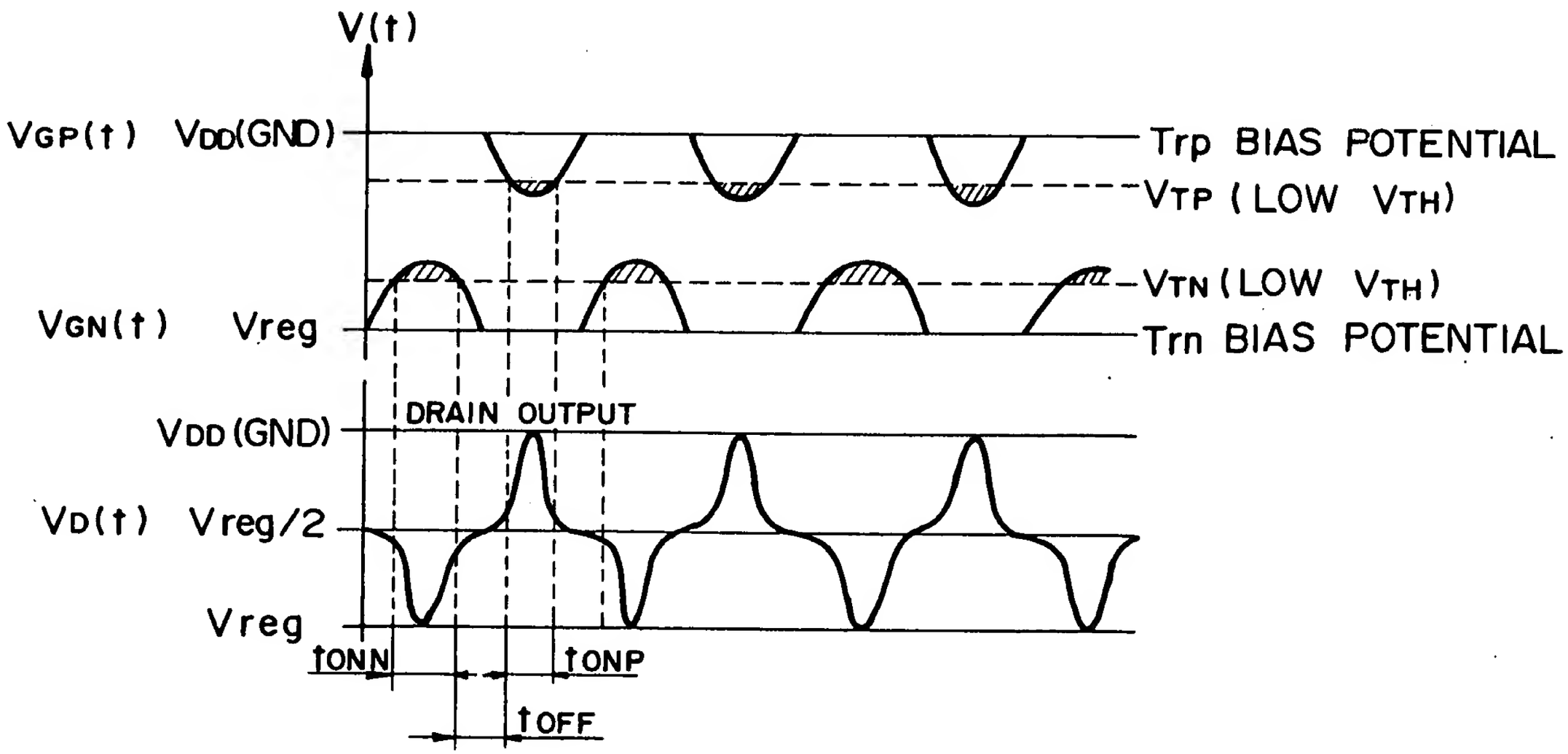

70
74
R_1
V_{DD} (GND)
42
30
72
Trp
$V_{GP}(t)$
$V_D(t)$
79
$V_{GN}(t)$
$V_G(t)$
Trn
82
84
R_2
52
80
Vreg
Vreg
10
14
C_G
16
18
C_D
V_{DD}
V_{DD}

FIG. 8



t_{ONN} : n-CHANNEL TRANSISTOR ON

t_{ONP} : p-CHANNEL TRANSISTOR ON

t_{OFF} : BOTH OF n-CHANNEL AND p-CHANNEL TRANSISTORS OFF

FIG. 9

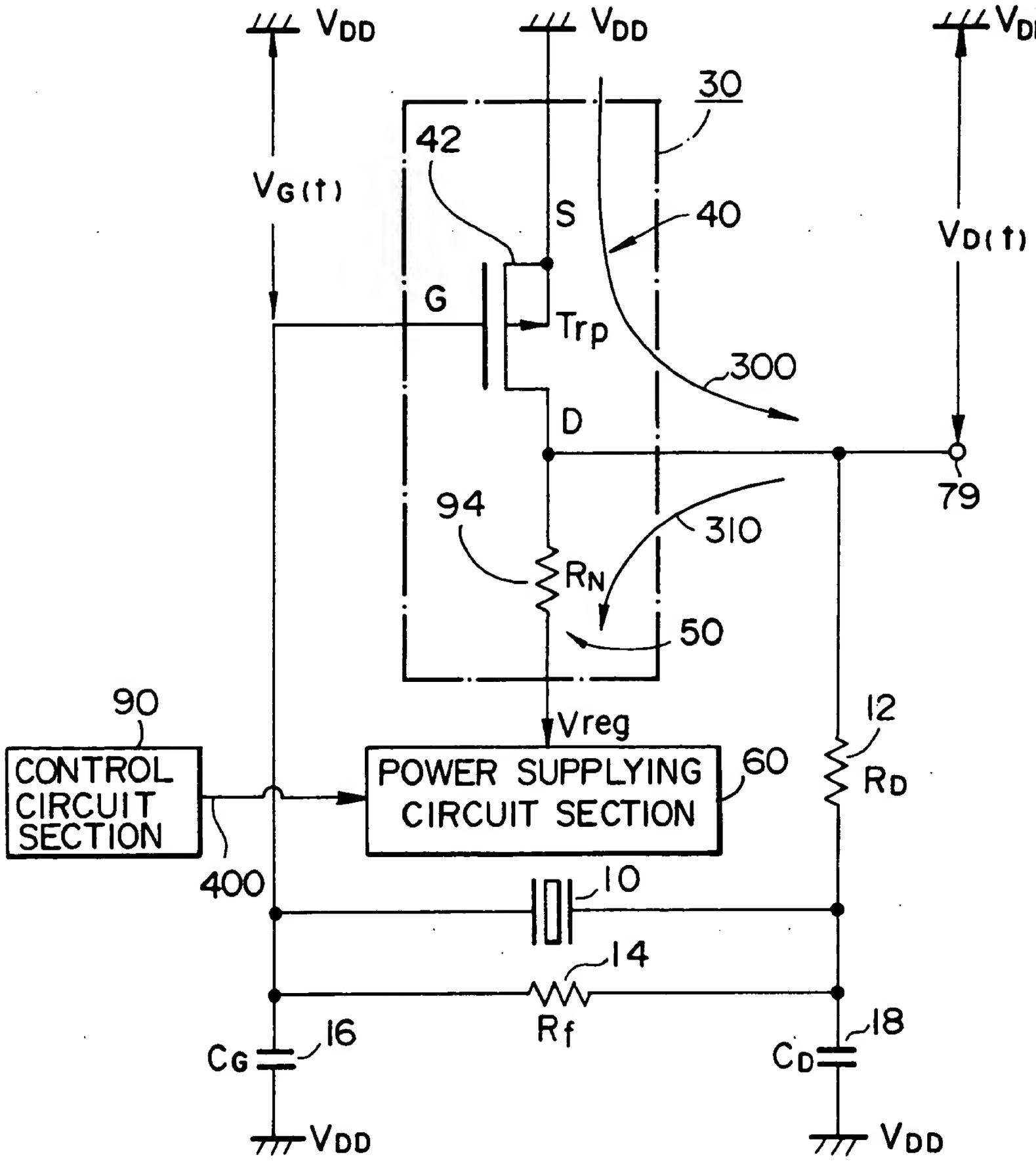

VDD
VDD
VDD
30
42
S
40
VG(t)
VD(t)
G
Trp
300
D
79
94
310
RN
50
90
Vreg
12
CONTROL CIRCUIT SECTION
POWER SUPPLYING CIRCUIT SECTION
60
RD
400
10
14
Rf
16
18
CG
CD
VDD
VDD

FIG. 10

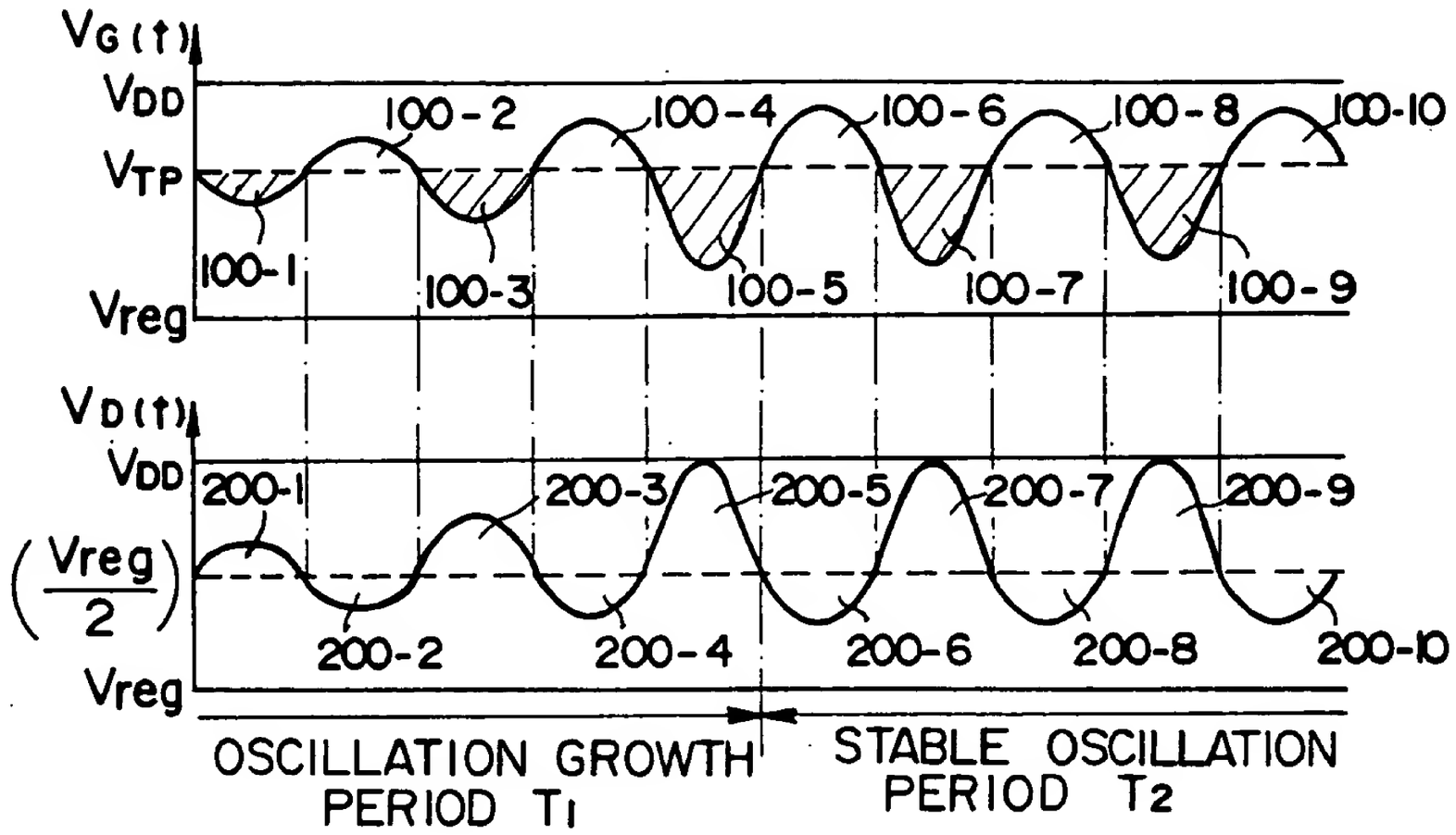

VG(t)
VDD
VTP
Vreg
100-1
100-2
100-3
100-4
100-5
100-6
100-7
100-8
100-9
100-10
VD(t)
VDD
(Vreg/2)
Vreg
200-1
200-2
200-3
200-4
200-5
200-6
200-7
200-8
200-9
200-10
OSCILLATION GROWTH PERIOD T1
STABLE OSCILLATION PERIOD T2

FIG. 11

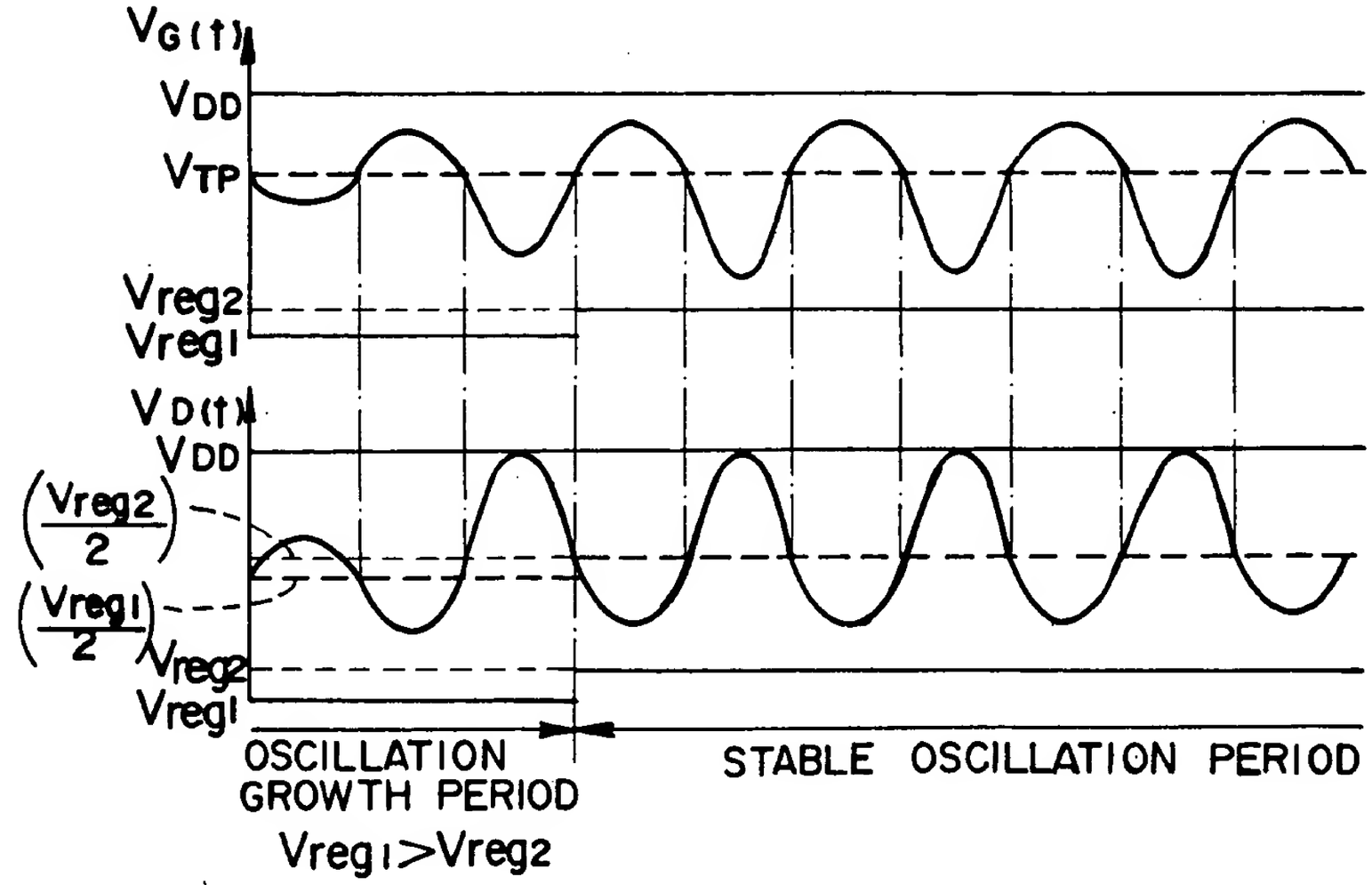

VG(t)
VDD
VTP
Vreg2
Vreg1
VD(t)
VDD
(Vreg2/2)
(Vreg1/2)
Vreg2
Vreg1
OSCILLATION GROWTH PERIOD
STABLE OSCILLATION PERIOD
Vreg1>Vreg2

FIG. 12

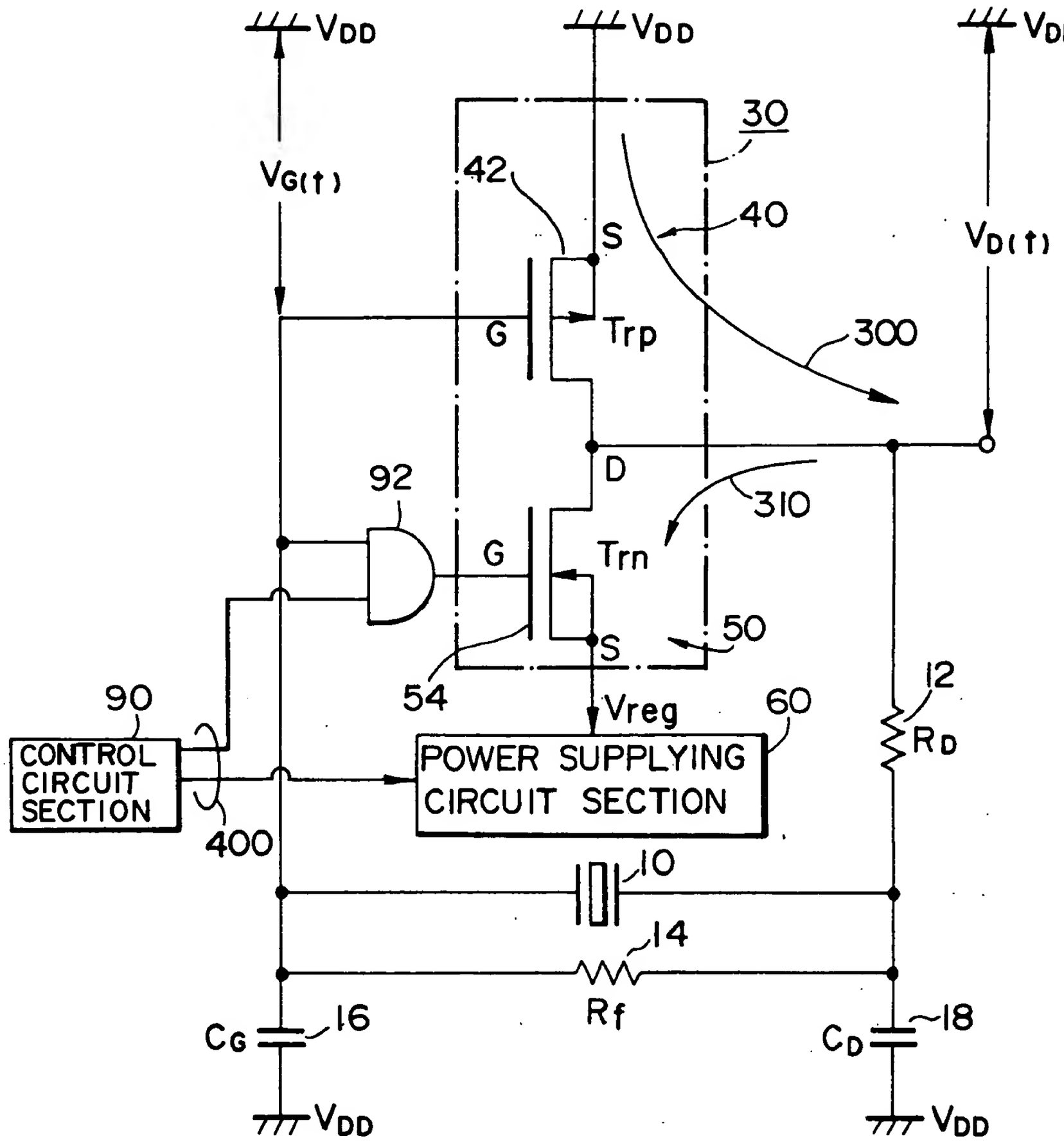

VDD
VDD
VDD
30
42
40
S
VG(t)
VD(t)
G
Trp
300
D
92
310
G
Trn
S
50
54
12
90
Vreg
60
CONTROL CIRCUIT SECTION
POWER SUPPLYING CIRCUIT SECTION
RD
400
10
14
Rf
CG
16
CD
18
VDD
VDD

FIG. 13

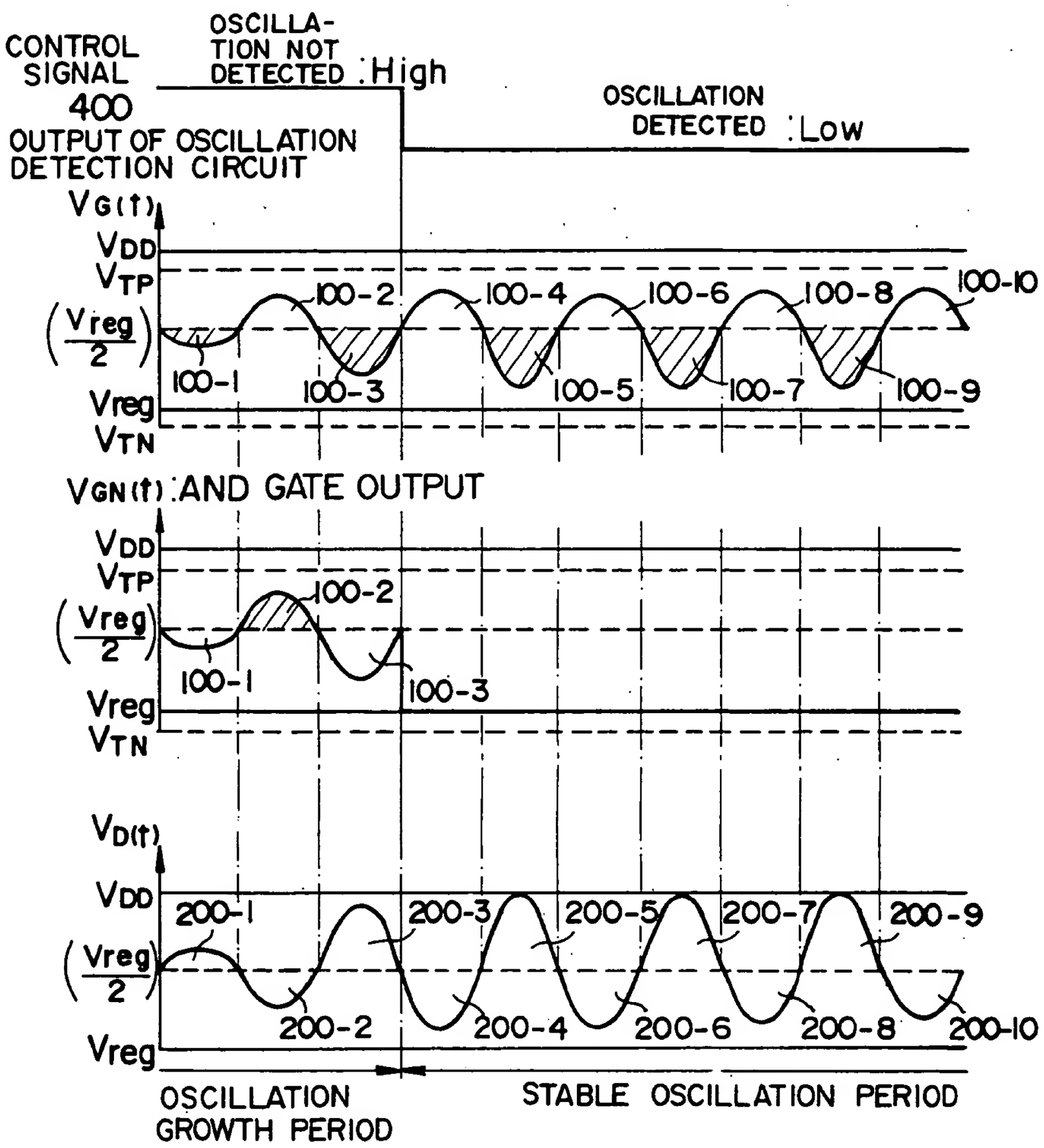

CONTROL SIGNAL 400
OSCILLATION NOT DETECTED : High
OSCILLATION DETECTED : Low
OUTPUT OF OSCILLATION DETECTION CIRCUIT
VG(t)
VDD
VTP
(Vreg/2)
Vreg
VTN
100-1
100-2
100-3
100-4
100-5
100-6
100-7
100-8
100-9
100-10
VGN(t) : AND GATE OUTPUT
VD(t)
200-1
200-2
200-3
200-4
200-5
200-6
200-7
200-8
200-9
200-10
OSCILLATION GROWTH PERIOD
STABLE OSCILLATION PERIOD

FIG. 14

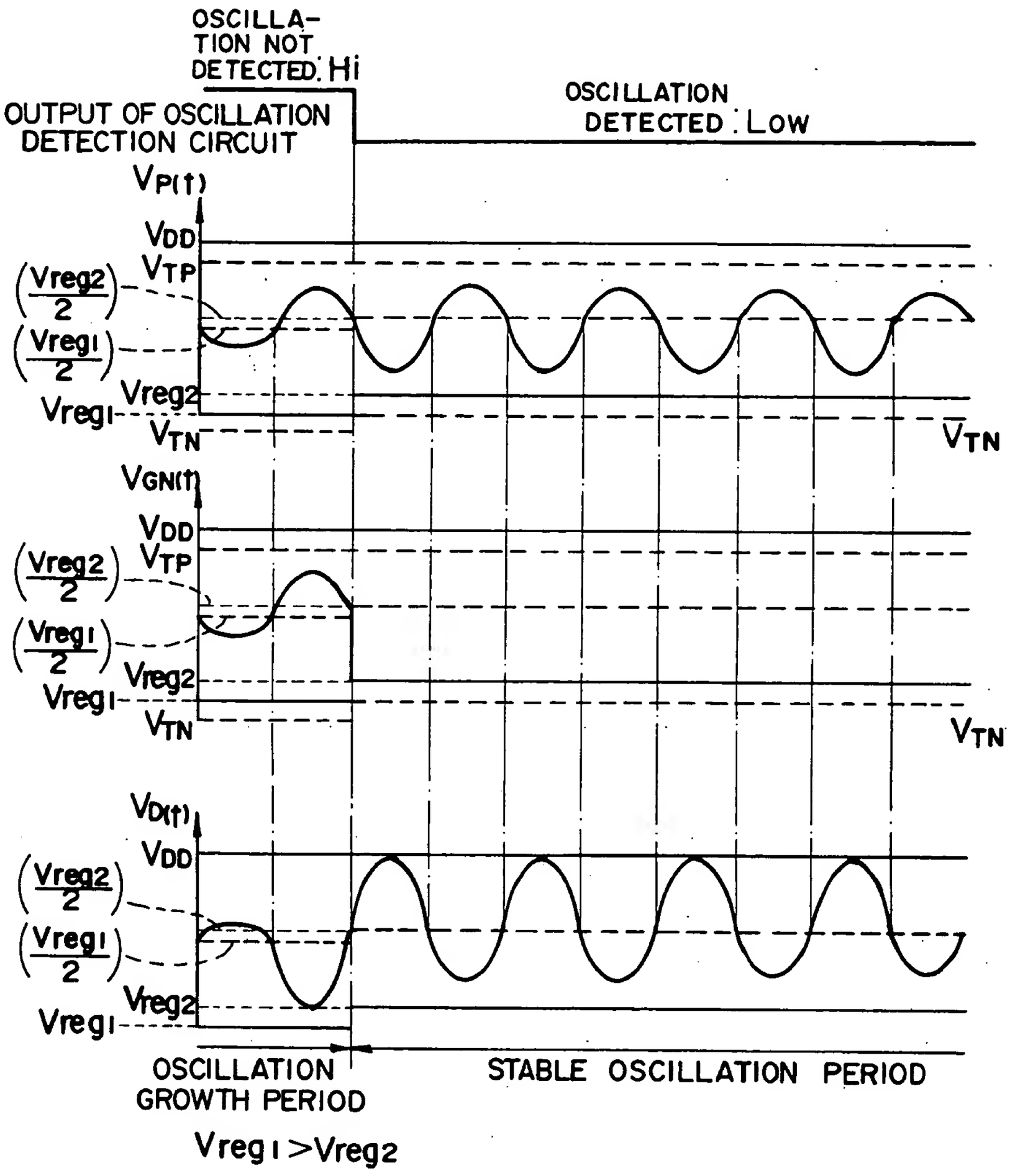

OSCILLATION NOT DETECTED : Hi
OSCILLATION DETECTED : Low
OUTPUT OF OSCILLATION DETECTION CIRCUIT
VP(t)
VDD
VTP
(Vreg2/2)
(Vreg1/2)
Vreg2
Vreg1
VTN
VGN(t)
VD(t)
OSCILLATION GROWTH PERIOD
STABLE OSCILLATION PERIOD
Vreg1 > Vreg2

FIG. 15

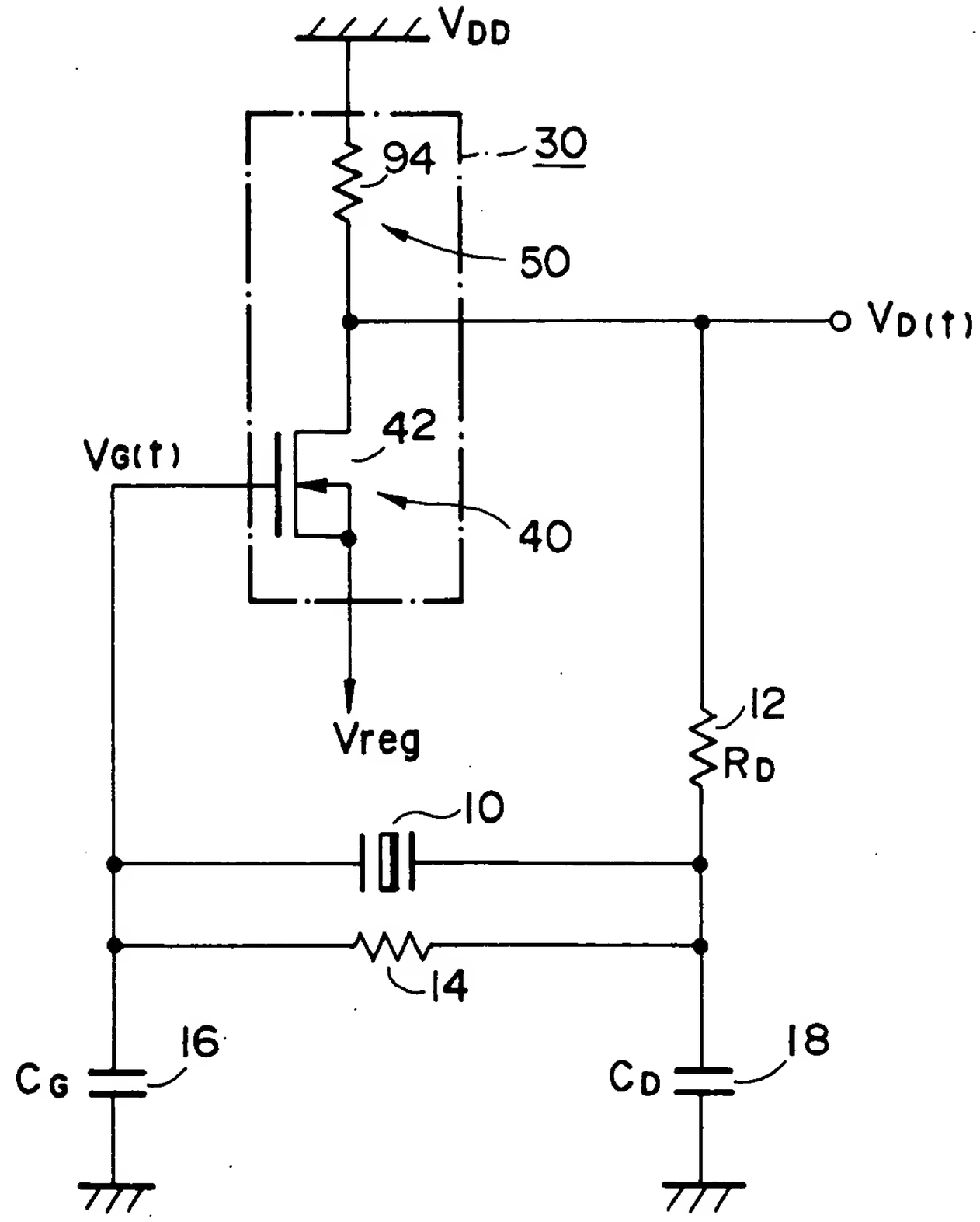


FIG. 16

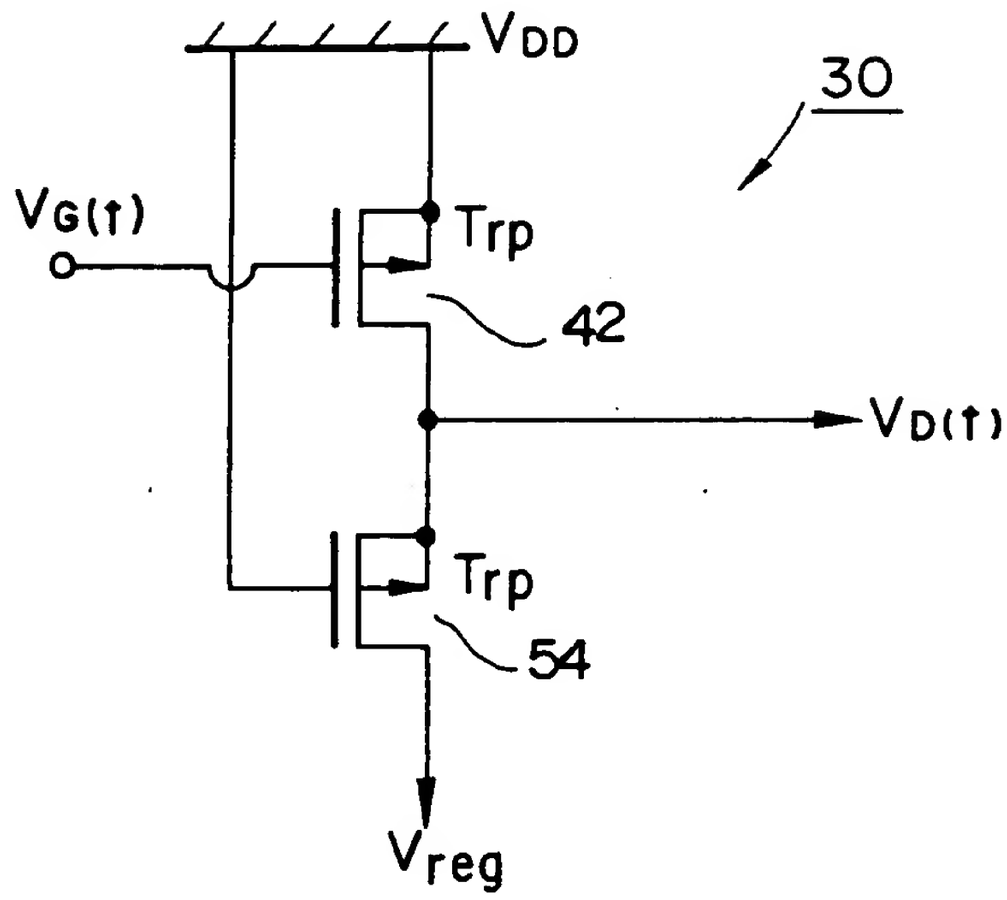

VDD
30
VG(t)
Trp
42
VD(t)
Trp
54
Vreg

FIG. 17

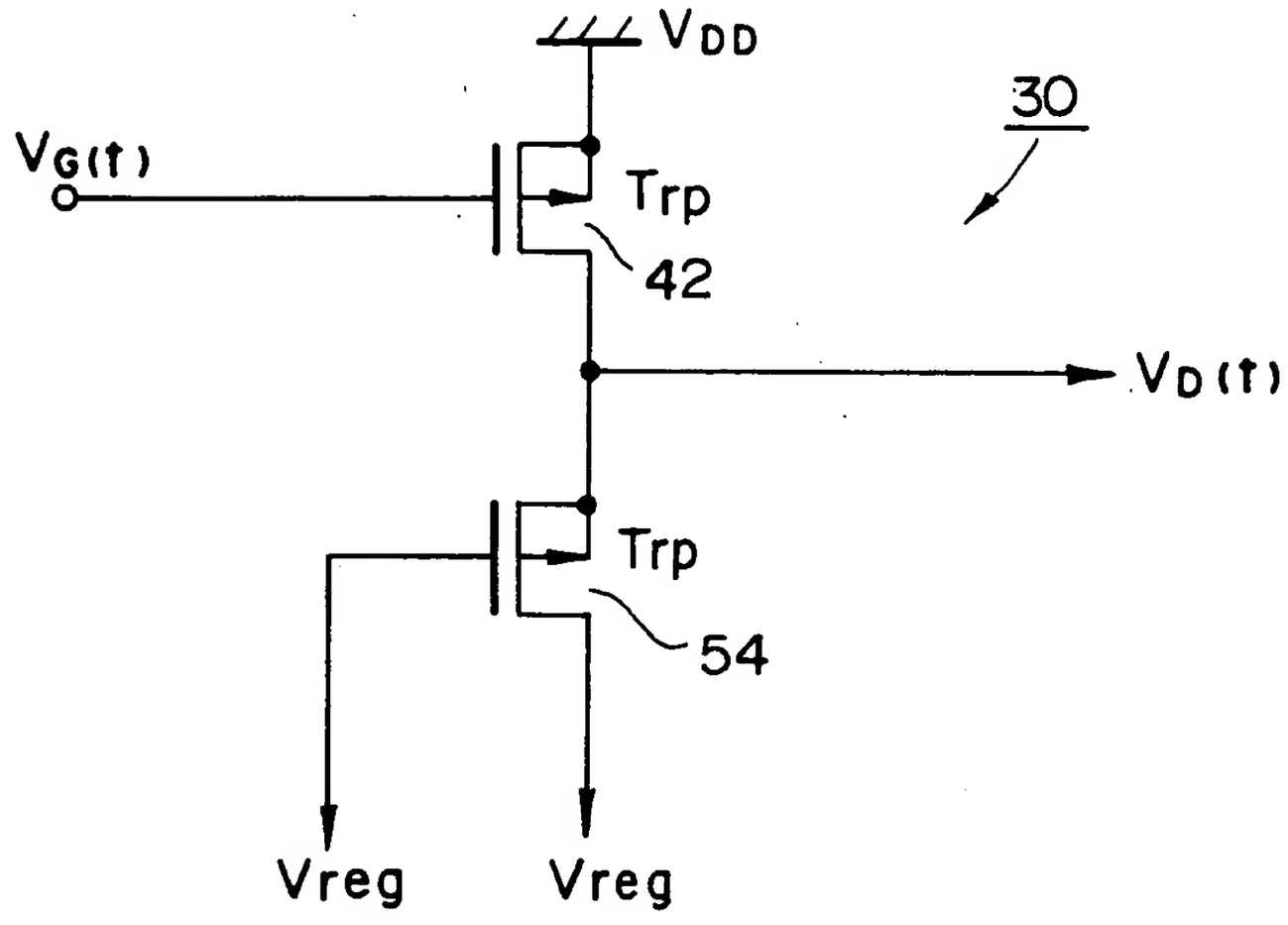

VDD
30
VG(t)
Trp
42
VD(t)
Trp
54
Vreg
Vreg

FIG. 18

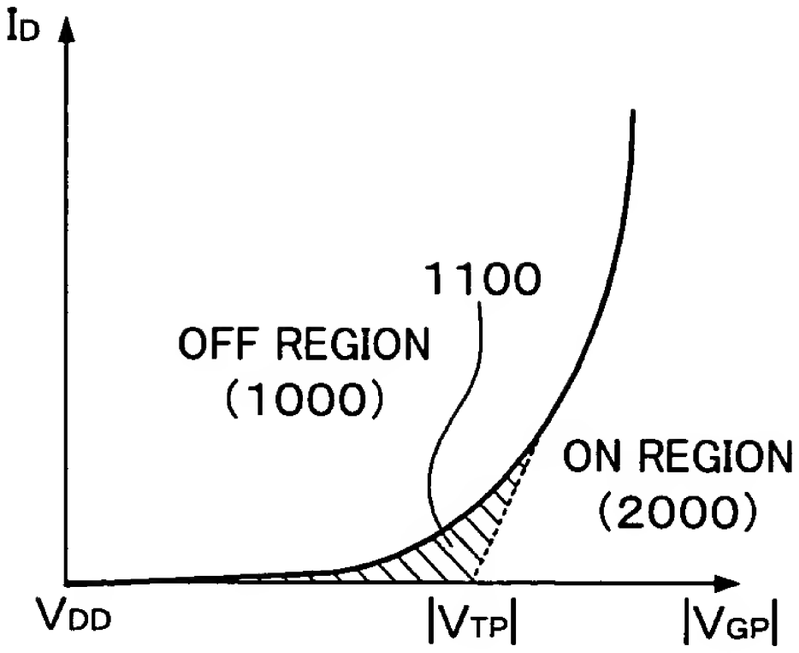

ID
1100
OFF REGION
(1000)
ON REGION
(2000)
VDD
|VTP|
|VGP|

FIG. 19

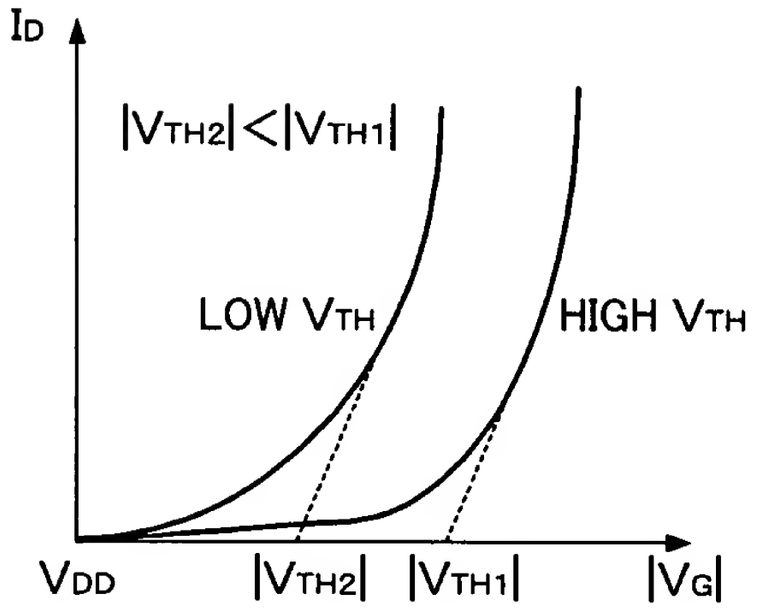

ID
|VTH2|<|VTH1|
LOW VTH
HIGH VTH
VDD
|VTH2|
|VTH1|
|VG|

FIG. 20

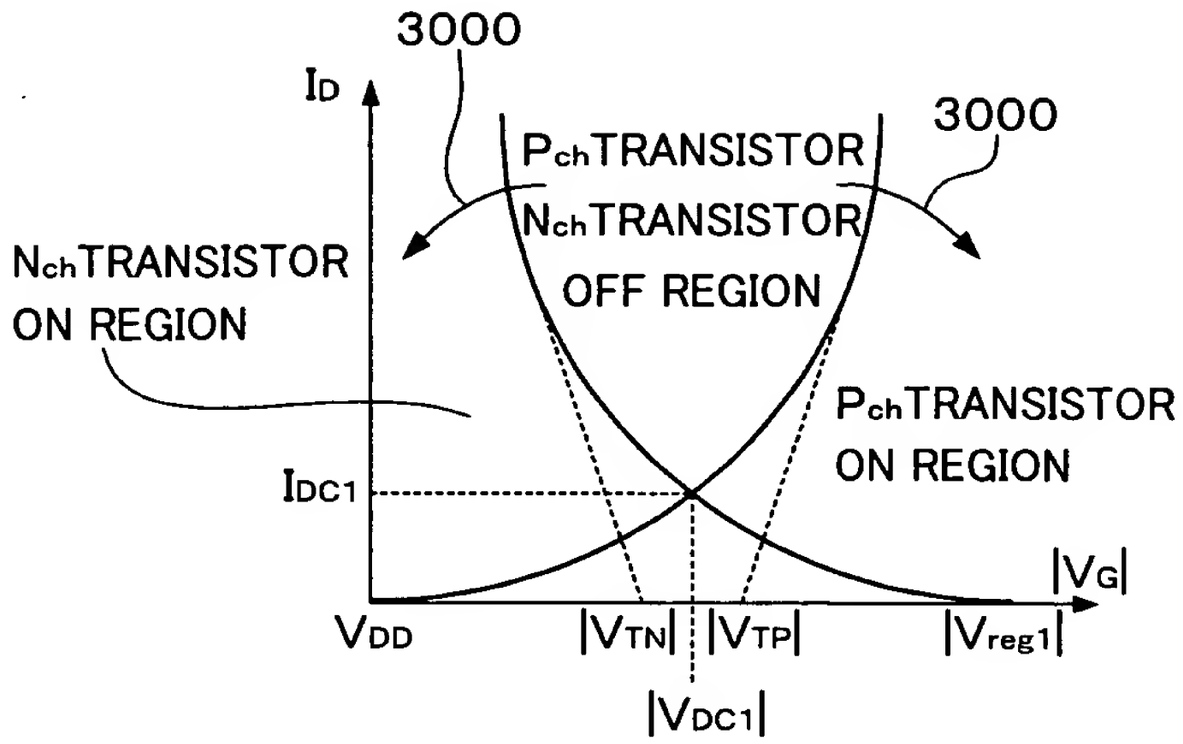

3000
ID
3000
PchTRANSISTOR
NchTRANSISTOR
OFF REGION
NchTRANSISTOR
ON REGION
PchTRANSISTOR
ON REGION
IDC1
|VG|
VDD
|VTN|
|VTP|
|Vreg1|
|VDC1|

FIG. 21

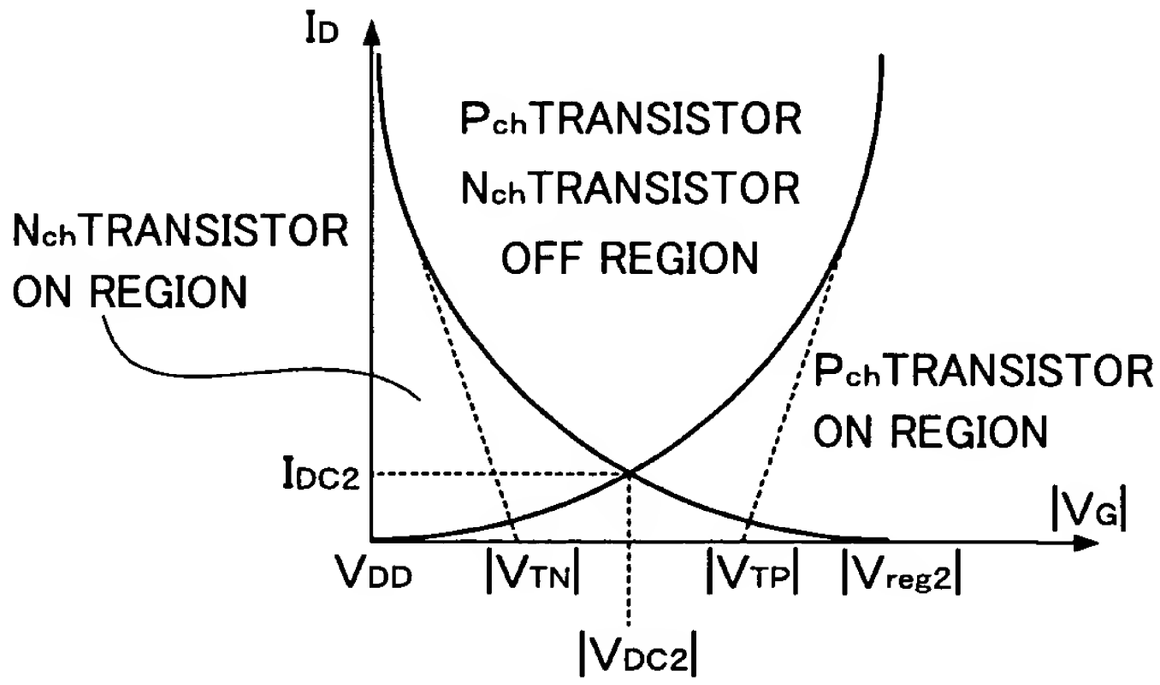

ID
PchTRANSISTOR
NchTRANSISTOR
OFF REGION
NchTRANSISTOR
ON REGION
PchTRANSISTOR
ON REGION
IDC2
|VG|
VDD
|VTN|
|VTP|
|Vreg2|
|VDC2|

FIG. 22

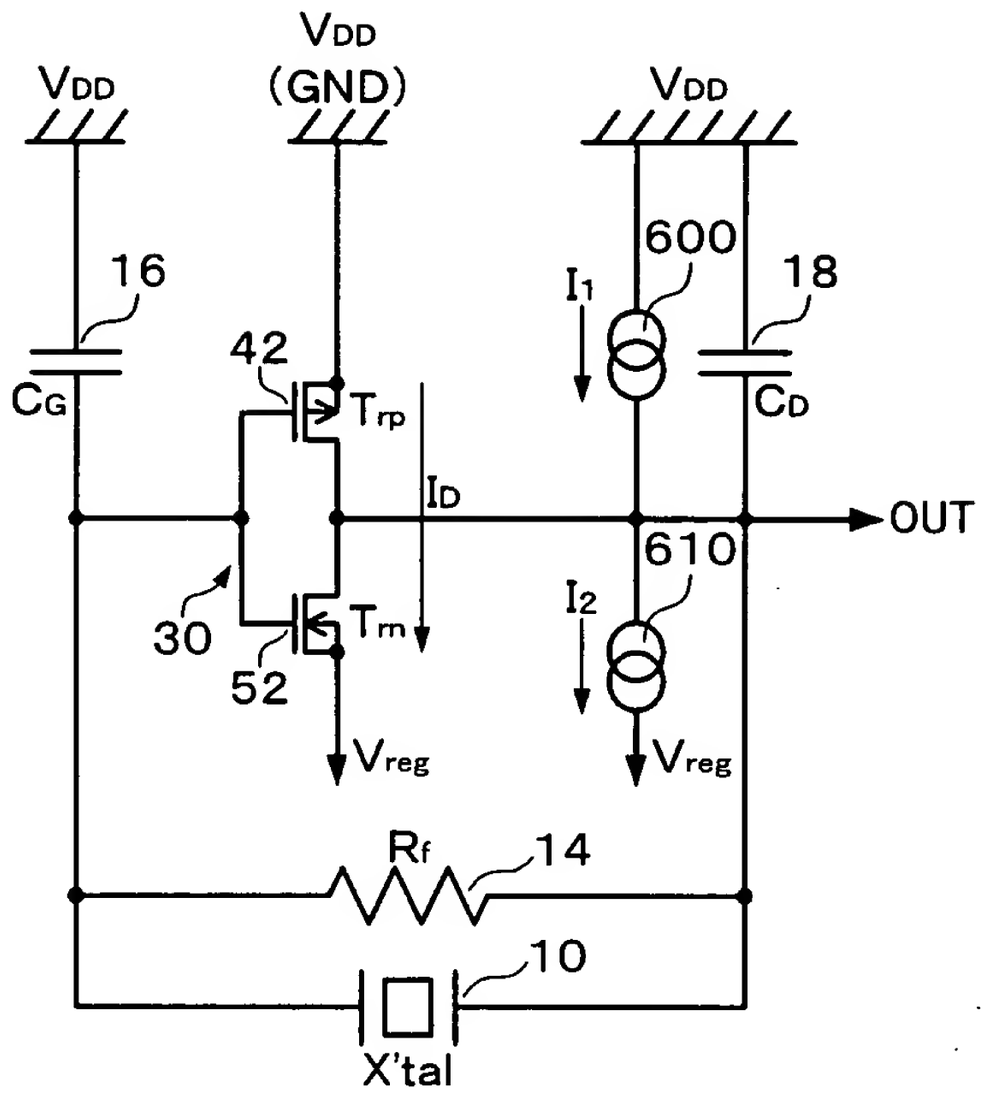
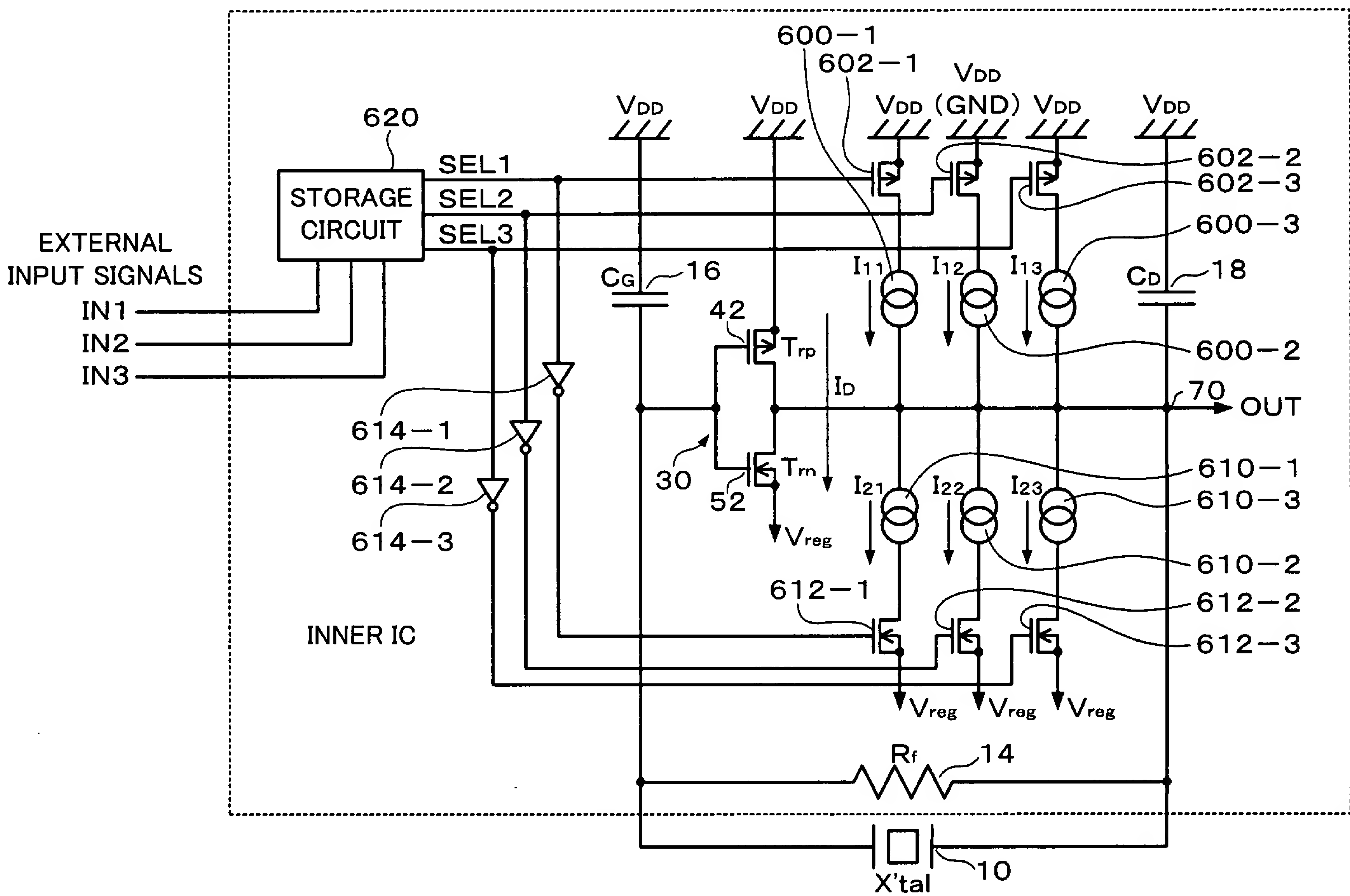

VDD
VDD
(GND)
VDD
16
600
18
I1
42
CG
Trp
CD
ID
OUT
610
30
Tm
I2
52
Vreg
Vreg
Rf
14
10
X'tal

FIG. 23



EXTERNAL INPUT SIGNALS
IN1
IN2
IN3
620
STORAGE CIRCUIT
SEL1
SEL2
SEL3
INNER IC
614−1
614−2
614−3
VDD
CG
16
42
Trp
30
52
Trn
Vreg
ID
600−1
602−1
VDD (GND)
602−2
602−3
600−3
600−2
I11
I12
I13
CD
18
70
OUT
610−1
610−3
610−2
I21
I22
I23
612−1
612−2
612−3
Rf
14
X'tal
10

FIG. 24

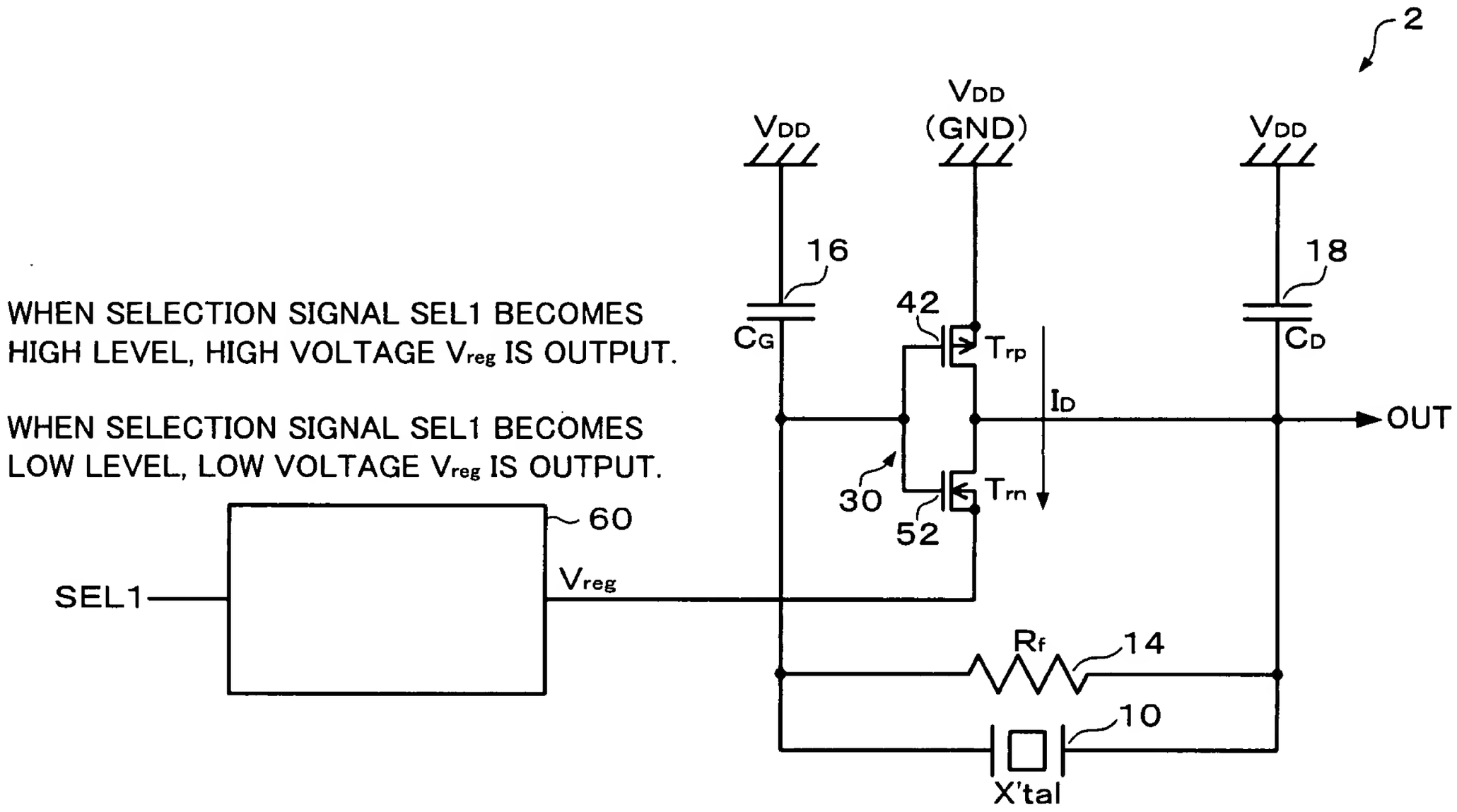

WHEN SELECTION SIGNAL SEL1 BECOMES HIGH LEVEL, HIGH VOLTAGE Vreg IS OUTPUT.
WHEN SELECTION SIGNAL SEL1 BECOMES LOW LEVEL, LOW VOLTAGE Vreg IS OUTPUT.
SEL1
60
Vreg
VDD
(GND)
VDD
VDD
16
18
42
CG
CD
Trp
Trn
ID
30
52
OUT
Rf
14
10
X'tal
2

FIG. 25

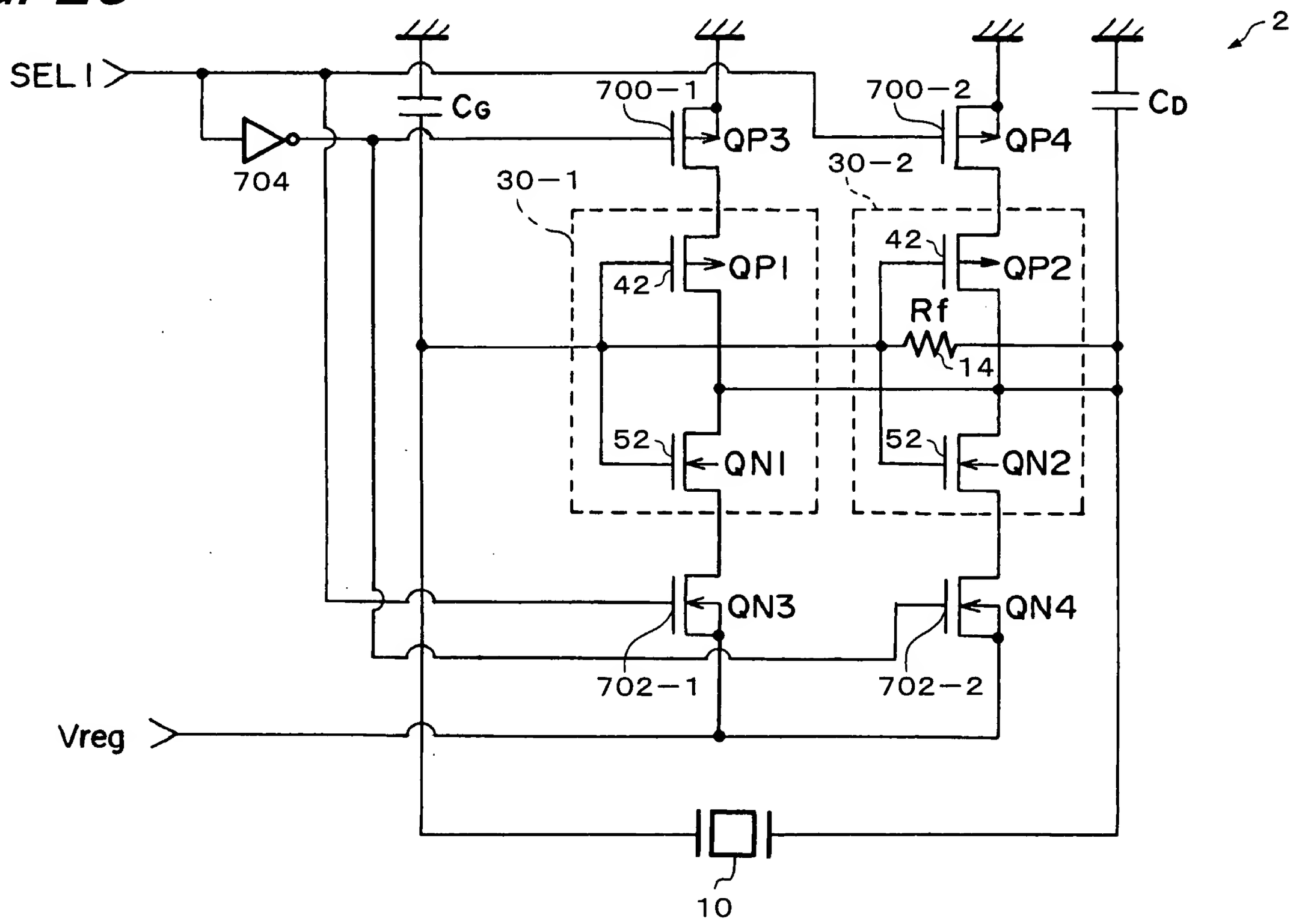

SEL I
704
CG
700−1
QP3
700−2
QP4
CD
2
30−1
30−2
42
QP1
42
QP2
Rf
14
52
QN1
52
QN2
QN3
QN4
702−1
702−2
Vreg
10

FIG. 26A

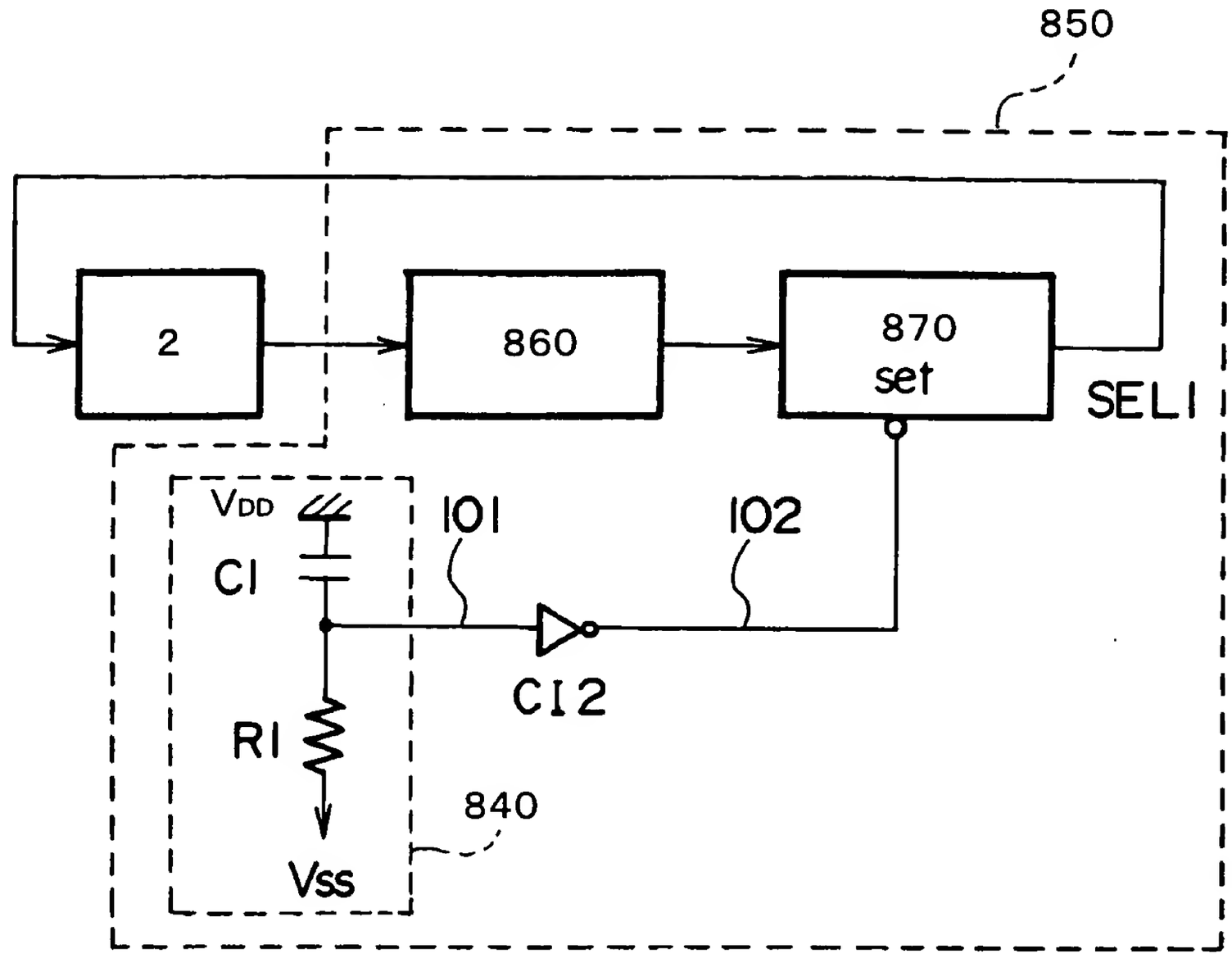


FIG. 26B

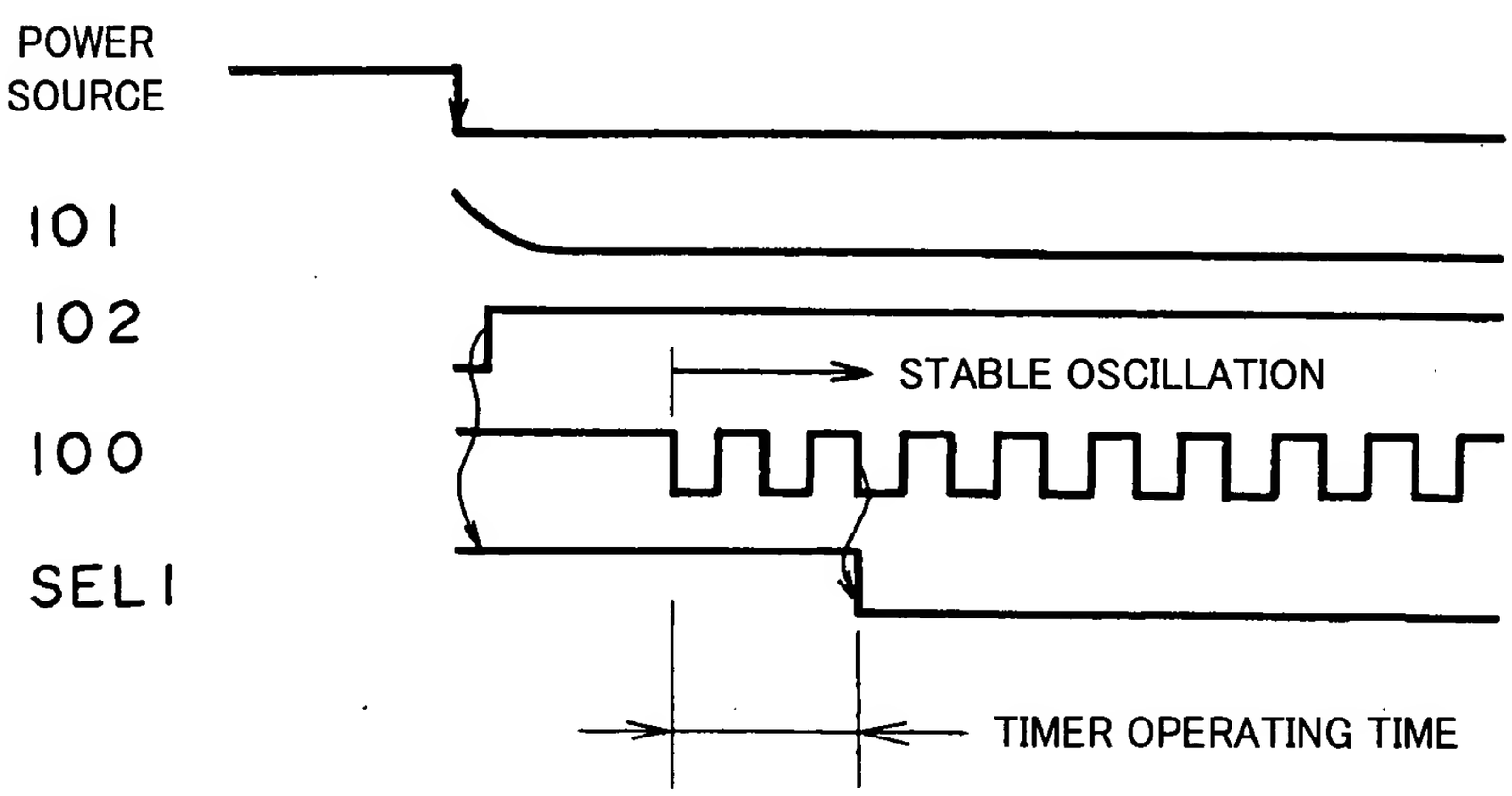


FIG. 27A

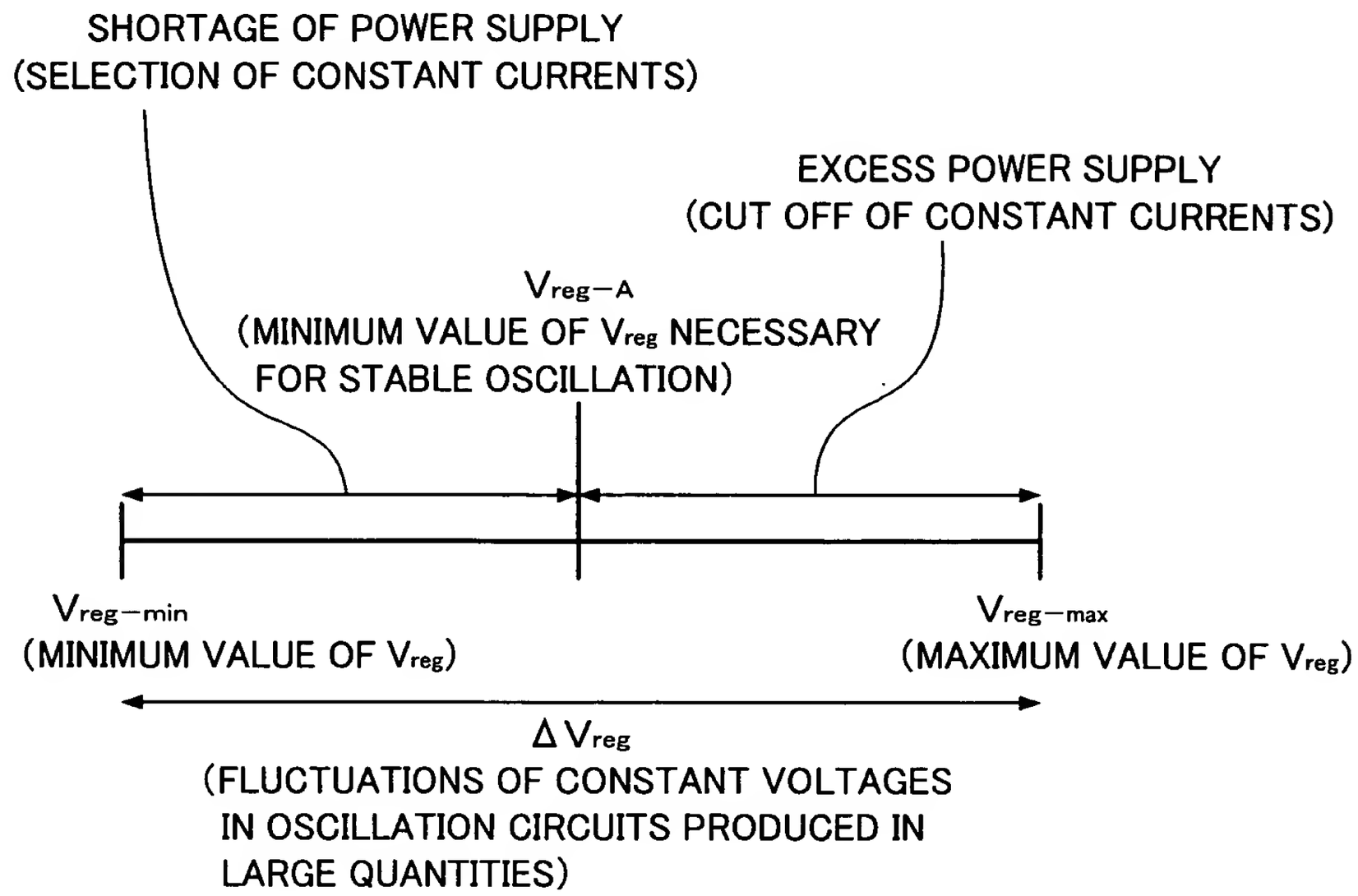


FIG. 27B